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Let's Get start Now. Enjoy & Stay connected with us... Hii.. How are you? First of All, Thanks for Watching My Video. I hope you like my content make sure to share it with Your Family, Friends and put Like & Subscribe button if you don't share it. Thank you Guys. Stay Tuned with us. I will be back with more cool content. 1. Field of the Invention The present invention relates to a circuit for generating a clock signal in which an edge of the clock signal can be shifted left or right in order to adjust the operation of the circuit. 2. Description of the Prior Art Nowadays, integrated circuits, such as digital-to-analog converters (DACs) have been extensively used in communication apparatuses, such as digital subscriber lines (DSL). The digital-to-analog converter (DAC) receives a digital input signal and converts the digital input signal into an analog output signal, such that the data transmission can be implemented. Please refer to FIG. 1. FIG. 1 illustrates a conventional integrated circuit, comprising a data latch 12, a D-flip-flop (DFF) 14, and a clock generator 16. The data latch 12 receives a digital input signal 102 and the data latch 12 provides the digital input signal 102 to the DFF 14 in response to the clock signal 116. The digital input signal 102 is provided to the DFF 14 generates the analog output signal 104. For example, assuming the output signal 104 has a voltage level between 0V and 5V, the output signal 104 is converted into the digital output signal 106 through the conversion of the voltage level. However, for a DSL communication, the clock frequency of the data rate of the DSL communication. In the conventional clock generator 16, only two clocks phases, that is, a rising edge and a falling edge, are provided. Thus, the clock frequency of the analog output signal is the same as the data rate, and cannot be adjusted according to the data rate of the DSL communication. Q: How to re-order a list to match a new order in the list of sublists I have the following 2